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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/887,793	06/22/2001	Richard W. Adkisson	10010788-1	7648

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EXAMINER	
CHEN, TSE W	
ART UNIT	**PAPER NUMBER**
2116	

DATE MAILED: 06/30/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/887,793	ADKISSON, RICHARD W.	
	Examiner	Art Unit	
	Tse Chen	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 June 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 11-29* is/are rejected.

7)☒ Claim(s) *2-10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. It is hereby acknowledged that the following papers have been received and placed of record in the file: Amendment dated June 3, 2005.

2. Claims 1-29 are presented for examination.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 11-14, 19-20, 22-24, and 28-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Magro et al., U.S. Patent 6516362, hereinafter Magro, in view of Watanabe, U.S. Publication 2002/0009169.

5. In re claim 1, Magro taught a system [microcontroller M] for synchronizing a first circuit portion [CPU 104] operating in a first clock domain that is clocked with a first clock signal [clk cpu 106] and a second circuit portion [SDRAM controller 102] operating in a second clock domain that is clocked with a second clock signal [clk mem 110] [fig.2a; abstract], comprising:

- Means for generating a sync pulse signal [phase sync 206] based on occurrence of a coincident edge between a first and second clock signals [fig.3b; col.8, ll.6-48; phase sync is generated when both clocks are in phase, i.e., coincident edge as shown in fig.3b, in order for timing of communication to work properly], said sync pulse signal comprising a sync pulse for every N [1] clock cycles of said first clock signal [fig.3b; phase_sync repeats for every N=1 clock cycle of clk_cpu].

- A clock synchronizer controller [SDRAM controller 102] operable to generate a plurality of control signals based on sync pulse signal [col.6, l.54 – col.7, l.5], said clock synchronizer controller including a sync adjuster [clock synchronizer logic 202] operable to re-position said sync pulse signal based on a coincident edge between said first and second clock signals defined in response to a skew between said first and second clock signals [fig.4, 5; col.8, l.39 – col.10, l.49; phase sync is automatically re-positioned in response to skew since it is generated in the same domain in which the determination of the skew is derived], wherein at least a portion of said plurality of control signals [data start, data end, etc.] actuate data transfer synchronizer circuitry disposed between said first and second circuit portions [col.7, l.52 – col.8, l.5; col.12, ll.29-50].

6. Magro did not discuss re-positioning the sync pulse based on a *new* coincident edge between the first and second clock signals defined in response to a skew between the first and second clock signals.

7. However, it would have been obvious to one of ordinary skill in the art to recognize that the sync adjuster can be modified to include a re-positioning of the sync pulse based on a new coincident edge between the first and second clock signals defined in response to a skew between the first and second clock signals in order to improve system performance by further removing any skew possible in the communication process [Watanabe: paragraph 0012-0014]. One of ordinary skill in the art would have been motivated to make such a modification as it provides a way to improve system performance [Watanabe: abstract].

8. In re claim 11, Magro discloses a method of synchronizing data transfer operations between two circuit portions across a clock domain boundary [abstract]:

- Generating a secondary clock signal from a primary clock signal [pll 108], wherein said primary clock signal [clk cpu 106] is operable to clock a first circuit portion [cpu 104] and said secondary clock signal [clk mem 110] is operable to clock a second circuit portion [SDRAM controller 102] [fig.2b].
- Generating a sync pulse signal [phase sync 206] based on occurrence of a coincident edge between said primary and secondary clock signals [fig.3b; col.8, ll.6-48; phase sync is generated when both clocks are in phase, i.e., coincident edge as shown in fig.3b, in order for timing of communication to work properly], said sync pulse signal comprising a sync pulse for every N [1] clock cycles of said primary clock signal [fig.3b; phase_sync repeats for every N=1 clock cycle of clk_cpu].
- Adjusting said sync pulse signal to re-position it based on a coincident edge that is defined responsive to a skew between said primary and secondary clock signals [fig.4, 5; col.8, l.39 – col.10, l.49; phase sync is automatically re-positioned in response to skew since it is generated in the same domain in which the determination of the skew is derived].
- Generating data transfer control signals at appropriate times relative to said primary and secondary clock signals [col.7, ll.59-66; col.12, ll.33-50] based on said sync pulse signal [col.9, ll.53-67] to control data transfer operations between said first and second circuit portions.

9. Magro did not discuss re-positioning the sync pulse based on a *new* coincident edge between the first and second clock signals defined in response to a skew between the first and second clock signals.

10. However, it would have been obvious to one of ordinary skill in the art to recognize that the sync adjuster can be modified to include a re-positioning of the sync pulse based on a new coincident edge between the first and second clock signals defined in response to a skew between the first and second clock signals in order to improve system performance by further removing any skew possible in the communication process [Watanabe: paragraph 0012-0014]. One of ordinary skill in the art would have been motivated to make such a modification as it provides a way to improve system performance [Watanabe: abstract].

11. As to claims 12 and 22, Magro discloses the secondary clock signal that is generated by a phase-locked loop [pll 108] based on the primary clock signal [fig.2b].

12. As to claims 13 and 23, Magro discloses the sync pulse signal that is generated when a rising edge in the primary clock signal coincides with a rising edge in the secondary clock signal [col. 8, ll.30-36].

13. As to claims 14 and 24, Magro discloses the sync pulse signal that is corrected if the sync pulse signal has a select clock period difference with respect to the primary clock signal [col.10, ll.18-49].

14. In re claims 19-20 and 28-29, Magro and Watanabe disclose each and every limitation as discussed above in reference to claims 11 and 21. In particular, Magro discloses a synchronizer for transferring data between two different clock domains. However, Magro did not disclose expressly the source for the two different clocks.

15. It would have been obvious to an ordinary artisan to utilize a core clock for the primary clock signal and a bus clock for the secondary clock signal because Applicant has not disclosed an advantage, a particular purpose, or solution to a stated problem for each of the respective

clock source. One of ordinary skill in the art, furthermore, would have expected Applicant's invention to perform equally well with other clock sources because the Applicant's invention is intended to synchronize two different clock signals, irrelevant of their generating sources.

16. Therefore, it would have been obvious to one of ordinary skill in the art to use a core clock for the primary clock signal and a bus clock for the secondary clock signal to obtain the invention as specified in claims 19 and 20.

17. Claims 15-17, 21, and 25-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Magro and Watanabe as applied to claim 11 above, and further in view of Shin, U.S. Patent 6212249.

18. In re claim 15, Magro and Watanabe disclose each and every limitation of the claim as discussed above in reference to claim 11. Magro and Watanabe did not discuss the details of determining the phase difference between the primary and secondary clock signal.

19. Shin discloses a method of synchronizing data transfer operations between two circuit portions [abstract], comprising:

- Determining a state [I-III] indicative of a phase difference between a primary [reference clock] and secondary [window signal] clock signals [col.6, l.45 -- col.7, l.19].
- Redefining a new coincident rising edge with respect to the primary and secondary clock signals based on the state [col.7, l.30 -- col.9, l.3; a new coincident rising edge is redefined in order to read properly from the floppy disk].

20. It would have been obvious to one of ordinary skill in the art, having the teachings of Magro, Watanabe, and Shin before him at the time of the invention, to modify the system taught by Magro and Watanabe to include the teaching of Shin in order to obtain the method comprising

determining a state indicative of a phase difference between a primary and secondary clock signals and redefining a new coincident rising edge with respect to the primary and secondary clock signals based on the state. One of ordinary skill in the art would have been motivated to make such a modification as it provides a way to maintain system stability [Shin: col.2, ll.7-37].

21. As to claims 16 and 25, Shin discloses the method wherein the new coincident rising edges with respect to the primary and secondary clock signals are redefined by adding at least an extra clock cycle when the state [decrement change DC] indicates that the primary clock signal lags with respect to the secondary clock signal by a predetermined amount [col.8, ll.53-62].

22. As to claims 17 and 26, Shin discloses the method wherein the new coincident rising edges with respect to the primary and secondary clock signals are redefined by deleting at least an extra clock cycle when the state [increment change IC] indicates that the primary clock signal lags with respect to the secondary clock signal by a predetermined amount [col.8, ll.39-52].

23. In re claim 21, Magro discloses a method of synchronizing data transfer operations between two circuit portions [CPU 104 and SDRAM controller 102] across a clock domain boundary [fig.2a; abstract], comprising:

- Generating a sync pulse signal [phase sync 206] based on occurrence of a coincident edge between a primary clock signal [clk cpu 106] operable with a first clock domain and a secondary clock signal [clk mem 110] operable with a second clock domain [fig.3b; col.8, ll.6-48; phase sync is generated when both clocks are in phase, i.e., coincident edge as shown in fig.3b, in order for timing of communication to work properly], said sync pulse signal comprising a sync pulse for every N [1] clock cycles of said primary clock signal [fig.3b; phase_sync repeats for every N=1 clock cycle of clk_cpu].

- Compensating for a skew between the primary and secondary clock signals and adjusting the sync pulse signal to re-position it based on the skew, *if necessary*, [fig.4, 5; col.8, l.39 – col.10, l.49; phase sync is automatically re-positioned in response to skew, if necessary, since it is generated in the same domain in which the determination of the skew is derived].
- Generating data transfer control signals [data start, data end, etc.] at appropriate times relative to said primary and secondary clock signals based on said sync pulse signal [col.6, l.54 – col.7, l.5] to control data transfer operations between said two circuit portions [col.7, l.52 – col.8, l.5; col.12, ll.29-50].

24. Magro did not discuss re-positioning the sync pulse based on a new coincident edge between the first and second clock signals defined in response to a skew between the first and second clock signals or the details of determining the phase difference between the primary and secondary clock signal.

25. In regards to the re-positioning of the sync pulse based on a new coincident edge, it would have been obvious to one of ordinary skill in the art to recognize that the sync adjuster can be modified to include a re-positioning of the sync pulse based on a new coincident edge between the first and second clock signals defined in response to a skew between the first and second clock signals in order to improve system performance by further removing any skew possible in the communication process [Watanabe: paragraph 0012-0014]. One of ordinary skill in the art would have been motivated to make such a modification as it provides a way to improve system performance [Watanabe: abstract].

26. In regards to the determining of the phase difference, Shin discloses a method of synchronizing data transfer operations between two circuit portions [abstract], comprising:

- Determining a state [I-III] indicative of a phase difference between a primary [reference clock] and secondary [window signal] clock signals [col.6, l.45 -- col.7, l.19].
- Redefining a new coincident rising edge with respect to the primary and secondary clock signals based on the state [col.7, l.30 -- col.9, l.3; a new coincident rising edge is redefined in order to read properly from the floppy disk].

27. It would have been obvious to one of ordinary skill in the art, having the teachings of Magro, Watanabe, and Shin before him at the time of the invention, to modify the system taught by Magro and Watanabe to include the teaching of Shin in order to obtain the method comprising compensating, if necessary, that includes determining a state indicative of a phase difference between a primary and secondary clock signals and redefining a new coincident rising edge with respect to the primary and secondary clock signals based on the state. One of ordinary skill in the art would have been motivated to make such a modification as it provides a way to maintain system stability [Shin: col.2, ll.7-37].

28. Claims 18 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Magro as applied to claims 11 and 21 above; and further in view of Csoppenszky et al, U.S. Patent 5987081, hereinafter Csoppenszky.

29. Magro taught a synchronizer for transferring data between two different clock domains by generating various data transfer control signals [col.6, ll.64-66] for the data transfer synchronizer circuitry [130] disposed between the first and second circuit portions [fig.2b].

30. However, Magro did not disclose expressly the details of configuration in which the data transfer control signals are transferred.

31. Csoppenszky taught a synchronizer for data transfer between clock domains [abstract], the synchronizer comprising of data transfer control signals that are staged through a plurality of registers [col.6, ll.7-36].

32. An ordinary artisan at the same time the invention was made would have been motivated to look for a stable way to transfer data in a system with two different clock domains [Csoppenszky: col.1, ll.11-45].

33. Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Magro and Csoppenszky because of the aforementioned motivation and also their involvement in similar problems regarding the synchronization of data transfer in a two-clock domain system.

Allowable Subject Matter

34. Claims 2-10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

35. The following is a statement of reasons for the indication of allowable subject matter: the claims are allowable because none of the references cited, either alone or in combination discloses or renders obvious a system of claim 1 wherein the sync adjustor comprises "a SYNC correct block operable to receive said SYNC pulse signal via a SYNC distributor, said SYNC correct block for correcting said SYNC pulse signal if said SYNC pulse signal has a particular clock period difference with respect to said first clock signal; a ratio detector coupled to said

SYNC correct block for detecting a frequency ratio relationship between said first and second clock signals; a state/correct block associated with a phase detector for determining a state indicative of a phase difference between said first and second clock signals, said state/correct block operating responsive to said frequency ratio relationship detected by said ratio detector; and a skew compensator operating responsive to said state to redefine said new coincident rising edge with respect to said first and second clock signals, whereby said SYNC pulse signal is re-aligned so as to correspond with said new coincident rising edges of said first and second clock signals".

Response to Arguments

36. Applicant's arguments, filed June 3, 2005, have been fully considered but they are not persuasive.

37. Applicant alleges that Magro "does not teach or suggest generating a sync pulse signal based on occurrence of a coincident edge between two clock signals wherein the sync pulse signal comprises a sync pulse for every N clock cycles of the first clock signal". Examiner disagrees as the rejection above and Applicant's admission that the "Magro reference is directed to... a synchronization signal called phase_sync signal 206 is generated that is identical to one of the clock signals..." demonstrates that Magro does teach the limitation [i.e., phase_sync signal inherently repeats for every N clock cycle since it is identical to one of the repeating clock signals].

38. Applicant alleges that Magro does not teach or suggest "adjusting the phase-sync signal 206 in order to re-position it based on a new coincident edge between the clk_mem and clk_cpu signals". Examiner disagrees as the rejection above demonstrates that Magro does teach or

suggest "adjusting the phase-sync signal 206 in order to re-position it based on a new coincident edge between the clk_mem and clk_cpu signals" [i.e., otherwise, Magro's invention would not operate effectively].

39. Applicant alleges that "there is no suggestion or motivation in either of the applied references to combine the teachings... Magro reference is concerned with skew between two clock signals ... Watanabe reference is concerned with skew between parallel data channels". Examiner disagrees as Applicant's admission demonstrates that both references are both involved with synchronization of skewed signals. Moreover, Applicant's admission that "Watanabe is concerned with... correcting the skew during the data transmission after correcting the skew by the first skew correct means" clearly supports Examiner's position that Watanabe provides irrefutable support/motivation for the teaching of adjusting the sync pulse signal in order to re-position it based on a new coincident edge between the first and second clock signals.

40. Applicant alleges that Magro and Watanabe "belong to different PTO classes ... any finding of motivation to combine the references is negatived". In response to applicant's argument that Magro and Watanabe are nonanalogous art, it has been held that a prior art reference must either be in the field of applicant's endeavor or, if not, then be reasonably pertinent to the particular problem with which the applicant was concerned, in order to be relied upon as a basis for rejection of the claimed invention. See *In re Oetiker*, 977 F.2d 1443, 24 USPQ2d 1443 (Fed. Cir. 1992). In this case, both references are involved in the field of data transmission systems and also involved with the problem of synchronizing skewed signals.

41. Applicant alleges that there "is no reasonable expectation of achieving success because of the requirement that the phase_sync signal of the Magro reference be generated only when there

is a fixed phase relationship between the two clock signals, which teaches away from variable phase differences in either direction between the reference clock and window signals as disclosed in the Shin reference". Examiner reminds Applicant that the phase_sync signal of Magro is generated when the ***phase***s of the two clock signals are ***sync***hronized [i.e., hence, the appropriately named phase_sync], not ***only*** when there is a fixed phase relationship between the two clock signals.

42. Generally, in response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Conclusion

43. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tse Chen whose telephone number is (571) 272-3672. The examiner can normally be reached on Monday - Friday 9AM - 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tse Chen
June 16, 2005

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